WHAT IS CLAIMED IS:

1. An integrated circuit structure, comprising:

a plurality of solid state electronic devices;

a plurality of conductive elements electrically coupling the electronic devices;

a dielectric layer positioned between two or more of the conductive elements; and

a liner comprising a compound including silicon and an element selected from the group consisting of carbon and nitrogen, the liner positioned between at least a portion of the dielectric layer and a conductive element.

2. The integrated circuit structure of Claim 1, wherein the liner is selected from the group consisting of silicon nitride, silicon oxy-nitride, silicon boron-nitride, silicon carbide, silicon oxy-carbide, and silicon boron-carbide.

3. The integrated circuit structure of Claim 1, wherein at least one of the conductive elements comprises a metallization line.

4. The integrated circuit structure of Claim 1, wherein at least one of the conductive elements comprises polysilicon.

5. The integrated circuit structure of Claim 1, wherein the dielectric layer comprises an intralevel dielectric layer positioned between conductive elements in a level of the integrated circuit structure.

6. The integrated circuit structure of Claim 1, wherein the dielectric layer comprises an interlevel dielectric layer positioned between conductive elements in different levels of the integrated circuit structure.

7. The integrated circuit structure of Claim 1, wherein the dielectric layer comprises a fluorinated dielectric material.

8. The integrated circuit structure of Claim 1, wherein the dielectric layer comprises polytetraflouroethylene (PTFE).

9. The integrated circuit structure of Claim 1, wherein the conductive elements are formed using a subtractive etch process.

10. The integrated circuit structure of Claim 1, wherein the conductive elements are formed using a damascene process.

11. An integrated circuit structure comprising a liner positioned between at least a portion of a dielectric layer and a conductive element, the liner comprising a compound including silicon and an element selected from the group consisting of carbon and nitrogen.

12. The integrated circuit structure of Claim 11, wherein the liner is selected from the group consisting of silicon nitride, silicon oxy-nitride, silicon boron-nitride, silicon carbide, silicon oxy-carbide, and silicon boron-carbide.

13. The integrated circuit structure of Claim 11, wherein the conductive element comprises a metallization line.

14. The integrated circuit structure of Claim 11, wherein the conductive element comprises polysilicon.

15. The integrated circuit structure of Claim 11, wherein the dielectric layer comprises an intralevel dielectric layer positioned between two or more conductive elements in a level of the integrated circuit structure.

16. The integrated circuit structure of Claim 11, wherein the dielectric layer comprises an interlevel dielectric layer positioned between two or more conductive elements in different levels of the integrated circuit structure.

17. The integrated circuit structure of Claim 11, wherein the dielectric layer comprises a fluorinated dielectric material.

18. A method of forming an integrated circuit structure, comprising:

forming a plurality of solid state electronic devices;

forming a plurality of conductive elements to electrically couple the electronic devices;

forming a dielectric layer between two or more of the conductive elements; and

forming a liner between at least a portion of the dielectric layer and a conductive element, the liner comprising a compound including silicon and an element selected from the group consisting of carbon and nitrogen.

19. The method of Claim 18, wherein the liner is selected from the group consisting of silicon nitride, silicon oxy-nitride, silicon boron-nitride, silicon carbide, silicon oxy-carbide, and silicon boron-carbide.

20. The method of Claim 18, wherein at least one of the conductive elements comprises a metallization line.

21. The method of Claim 18, wherein at least one of the conductive elements comprises polysilicon.

22. The method of Claim 18, wherein forming the dielectric layer comprises forming an intralevel dielectric layer between conductive elements in a level of the integrated circuit structure.

23. The method of Claim 18, wherein forming the dielectric layer comprises forming an interlevel dielectric layer between conductive elements in different levels of the integrated circuit structure.

24. The method of Claim 18, wherein the dielectric layer comprises a fluorinated dielectric material.

25. The method of Claim 18, wherein the dielectric layer comprises polytetraflouroethylene (PTFE).

26. The method of Claim 18, wherein the conductive elements are formed using a subtractive etch process.

27. The method of Claim 18, wherein the conductive elements are formed using a damascene process.